AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in this application:

Listing of Claims:

1. (Original) A non-volatile multi-stable memory device, comprising:

a first electrode;

a second electrode; and

a composite medium disposed between and in contact with the first and second electrodes;

wherein the composite medium comprises a layer of discrete charge trapping particles so that an electrical resistance measured across the first and second electrodes is selectively variable between a lower resistance R_{on} and a higher resistance R_{off};

wherein R_{on} is selected by applying a turn-on potential V_{on} between the first and second electrodes;

wherein R_{off} is selected by applying a turn-off potential V_{off} between the first and second electrodes;

wherein the absolute value of the turn-off potential, $|V_{off}|$, is greater than the absolute value of the turn-on potential, $|V_{on}|$; and

wherein the turn-off potential, V_{off} and the turn-on potential, V_{on} have the same polarity.

2. (Original) The memory device of claim 1, wherein the composite medium further comprises a layer of charge transporting semiconductor material in which the layer of discrete charge trapping particles is embedded, has a "primary band gap" between approximately 1.5 and 6 eV.

3. (Original) The memory device of claim 1, wherein the absolute value of the turn-on potential, $|V_{on}|$ is greater than the absolute value of a predetermined threshold potential, $|V_T|$ of the composite medium.

4. (Original) The memory device of claim 1, wherein the charge trapping particles comprise discrete atoms embedded in the layer of charge transporting material.

5. (Original) The memory device of claim 1, wherein the charge trapping particles comprise discrete ions embedded in the layer of charge transporting material.

6. (Original) The memory device of claim 1, wherein the charge trapping particles comprise discrete molecules embedded in the layer of charge transporting material.

7. (Original) The memory device of claim 1, wherein the charge trapping particles comprise discrete molecular clusters embedded in the layer of charge transporting material.

9. (Original) The memory device of claim 1, wherein the charge trapping particles are metallic.

10. (Original) The memory device of claim 2, wherein the charge trapping particles are semiconducting with a band gap less than the band gap of the charge transporting semiconductor material.

11. (Original) The memory device of claim 1, wherein the charge trapping particles comprise discrete nanoparticles embedded in the layer of charge transporting material.

12. (Original) The memory device of claim 1, wherein the layer of discrete charge trapping particles is separated from the electrodes by intermediate layers of charge transporting material.

13. (Original) The memory device of claim 1, wherein upon applying the turn-on potential V_{on} between the first electrode and the second electrode, substantially no charge is retained by the composite medium, and wherein a corresponding on state is maintained for at least 10 seconds.

14. (Original) The memory device of claim 1, wherein upon applying the turn-off potential V_{off} between the first electrode and the second electrode, the composite medium retains a charge with a charge dissipation decay time of at least 10 seconds.

15. (Original) The memory device of claim 1, wherein $|R_{on}|$ and $|R_{off}|$ differ by at least a factor of approximately 2.

16. (Original) The memory device of claim 2, wherein the charge transporting semiconductor material comprises an organic electron transport material.

17. (Original) The memory device of claim 16, wherein the organic electron transport material comprises aluminum triquinolate.

18. (Original) The memory device of claim 2, wherein the charge transporting semiconductor material comprises an organic hole transport material.

19. (Original) The memory device of claim 18, wherein the organic hole transport material is NPB.

20. (Original) The memory device of claim 2, wherein the charge transporting semiconductor material comprises a crosslinkable arylamine polymer.

21. (Original) The memory device of claim 20, wherein the arylamine polymer is HTPA.

22. (Original) The memory device of claim 2, wherein the charge transporting semiconductor material comprises is inorganic with a band gap greater than approximately 2 eV.

23. (Original) The memory device of claim 22, wherein the semiconductor is SiO.

24. (Original) The memory device of claim 2, where the charge trapping particles form a separate layer within the charge transporting semiconductor material.

25. (Original) The memory device of claim 2, where the charge trapping particles are dispersed in the charge transporting semiconductor material.

26. (Original) The memory device of claim 2, where the charge transporting semiconductor material comprises a plurality of layers; and

wherein at least one of the plurality of layers comprises a dispersion of charge storage particles.

27. (Original) A bistable switching element, comprising:

a first electrode;

a second electrode; and

a composite medium disposed between and in contact with the first and second electrodes;

wherein the composite medium comprises a layer of discrete charge trapping particles so that an electrical resistance measured across the first and second electrodes is selectively variable between a lower resistance R_{on} and a higher resistance R_{off};

wherein R_{on} is selected by applying a turn-on potential V_{on} between the first and second electrodes;

wherein R_{off} is selected by applying a turn-off potential V_{off} between the first and second electrodes;

wherein the absolute value of the turn-off potential, $|V_{off}|$, is greater than the absolute value of the turn-on potential, $|V_{on}|$; and

wherein the turn-off potential, V_{off} and the turn-on potential, V_{on} have the same polarity.

28. (Original) The bistable switching element of claim 27, wherein the composite medium further comprises a layer of charge transporting semiconductor material in which the layer of discrete charge trapping particles is embedded, has a "primary band gap" between approximately 1.5 and 6 eV.

29. (Original) The bistable switching element of claim 28, wherein the layer of charge transporting semiconductor material has a band gap that is greater that approximately 2 eV.

30. (Original) The bistable switching element of claim 27, wherein the charge trapping particles and the first electrode are selected so that charges of a predetermined polarity is allowed to be injected into the composite medium; and

wherein the charge trapping particles and the second electrode are selected so that charges of a opposite polarity are prevented from being injected into the composite medium.

31. (Original) The bistable switching element of claim 27, wherein the discrete trapping particles are distributed throughout the semiconductor material so that a maximum density of the discrete trapping particles is located nearly equidistantly between the first and second electrodes.

32. (Original) A memory system comprised of an array of non-volatile multi-stable memory devices, each memory device comprising:

a first electrode;

a second electrode; and

a composite medium disposed between and in contact with the first and second electrodes;

wherein the composite medium comprises a layer of discrete charge trapping particles so that an electrical resistance measured across the first and second electrodes is selectively variable between a lower resistance R_{on} and a higher resistance R_{off};

wherein R_{on} is selected by applying a turn-on potential V_{on} between the first and second electrodes;

wherein R_{off} is selected by applying a turn-off potential V_{off} between the first and second electrodes;

wherein the absolute value of the turn-off potential, $|V_{off}|$, is greater than the absolute value of the turn-on potential, $|V_{on}|$; and

wherein the turn-off potential, V_{off} and the turn-on potential, V_{on} have the same polarity.

33. (Original) A switching system comprised of an array of multi-stable switching elements, each element comprising:

a first electrode;

a second electrode; and

a composite medium disposed between and in contact with the first and second electrodes;

wherein the composite medium comprises a layer of discrete charge trapping particles so that an electrical resistance measured across the first and second electrodes is selectively variable between a lower resistance R_{on} and a higher resistance R_{off};

wherein R_{on} is selected by applying a turn-on potential V_{on} between the first and second electrodes;

wherein R_{off} is selected by applying a turn-off potential V_{off} between the first and second electrodes;

wherein the absolute value of the turn-off potential, $|V_{off}|$, is greater than the absolute value of the turn-on potential, $|V_{on}|$; and

wherein the turn-off potential, V_{off} and the turn-on potential, V_{on} have the same polarity.

34. (Original) The switching system of claim 33, wherein the composite medium further comprises a layer of charge transporting semiconductor material in which the layer of discrete charge trapping particles is embedded, has a "primary band gap" between approximately 1.5 and 6 eV.

35. (Original) The switching system of claim 34, wherein the layer of charge transporting semiconductor material has a band gap that is greater that approximately 2 eV.

36. (Original) The switching system of claim 33, wherein the charge trapping particles and the first electrode are selected so that charges of a predetermined polarity is allowed to be injected into the composite medium; and

wherein the charge trapping particles and the second electrode are selected so that charges of a opposite polarity are prevented from being injected into the composite medium.

37. (Original) The switching system of claim 33, wherein the discrete trapping particles are distributed throughout the semiconductor material so that a maximum density of the discrete trapping particles is located nearly equidistantly between the first and second electrodes.

38. (Withdrawn) A method of forming a non-volatile multi-stable memory device, comprising:

depositing a first electrically conductive layer onto a substrate to form a first electrode;

depositing a composite medium onto the first electrode; and

depositing a second electrically conductive layer onto the composite medium to form a second electrode;

wherein the composite medium comprises a layer of discrete charge trapping particles so that an electrical resistance measured across the first and second electrodes is selectively variable between a lower resistance R_{on} and a higher resistance R_{off};

wherein R_{on} is selected by applying a turn-on potential V_{on} between the first and second electrodes;

wherein R_{off} is selected by applying a turn-off potential V_{off} between the first and second electrodes;

wherein the absolute value of the turn-off potential, $|V_{off}|$, is greater than the absolute value of the turn-on potential, $|V_{on}|$; and

wherein the turn-off potential, V_{off} and the turn-on potential, V_{on} have the same polarity.

39. (Original) A method of using a non-volatile multi-stable memory device that includes a first electrode, a second electrode, and a composite medium disposed between and in contact with the first and second electrodes, wherein the composite medium comprises a layer of discrete charge trapping particles so that an electrical resistance measured across the first and second electrodes is selectively variable between a lower resistance R_{on} and a higher resistance R_{off}; the method comprising:

selecting the lower resistance R_{on} by applying a turn-on potential V_{on} between the first and second electrodes;

selecting the higher resistance R_{off} by applying a turn-off potential V_{off} between the first and second electrodes;

wherein the absolute value of the turn-off potential, $|V_{off}|$, is greater than the absolute value of the turn-on potential, $|V_{on}|$; and

wherein the turn-off potential, V_{off} and the turn-on potential, V_{on} have the same polarity.

40. (Original) The method of claim 39, further comprising reading a state of the multi-stable memory device by applying a reading voltage pulse.

41. (Original) A logical device comprising:

a first electrode;

a second electrode; and

a composite medium disposed between and in contact with the first and second electrodes;

wherein the composite medium comprises a layer of discrete charge trapping particles so that an electrical resistance measured across the first and second electrodes is selectively variable between a lower resistance R_{on} and a higher resistance R_{off};

wherein R_{on} is selected by applying a turn-on potential V_{on} between the first and second electrodes;

wherein R_{off} is selected by applying a turn-off potential V_{off} between the first and second electrodes;

wherein the absolute value of the turn-off potential, $|V_{off}|$, is greater than the absolute value of the turn-on potential, $|V_{on}|$; and

wherein the turn-off potential, V_{off} and the turn-on potential, V_{on} have the same polarity.